

# Claims

- [c1] 1. A gray-code error corrector comprising:
- an input for receiving input gray-code words in a received sequence, the input gray-code words belonging to a full sequence of gray-code values, wherein successive gray-code values in the full sequence have only one bit difference, wherein the received sequence contains successively-received words that differ by a maximum of  $N$  bits, wherein  $N$  is a whole number of two or more, wherein the successively-received words differ in value by a maximum of  $2^N - 1$ ,
  - a received register, coupled to receive an input gray-code word received by the input, the received register having an upper received-register that stores upper received bits and a lower received-register that stores  $N$  lower received bits of the input gray-code word;
  - a stored register that stores a corrected gray-code word, the stored register having an upper stored-register that stores upper stored bits and a lower stored-register that stores  $N$  lower stored bits of the corrected gray-code word;
  - an upper comparator, coupled to the received register and to the stored register, for comparing the upper re-

ceived bits to the upper stored bits;  
an upper loader, activated by the upper comparator when the upper received bits and the upper stored bits mis-match, for copying the upper received bits into the upper stored-register;  
a low-bit generator that generates lower stored bits for loading into the lower stored-register such that the stored register has a lowest-possible value within the full sequence of gray-code values after loading; and  
a full comparator, coupled to the received register and to the stored register, activated when the upper comparator determines that the upper received bits match the upper stored bits to compare the input gray-code word to the corrected gray-code word.

[c2] 2.The gray-code error corrector of claim 1 further comprising:

a differing-bit searcher, activated when the upper comparator determines that the upper received bits match the upper stored bits and when the full comparator determines that the input gray-code word is larger than the corrected gray-code word, for locating a first differing bit-position and loading bits above the first differing bit-position from the received register into the stored register and generating lowest-possible low bits for storage in the stored register below the first differing

bit-position;

wherein the low-bit generator generates the lowest-possible low bits such that upon loading with the lowest-possible low bits the stored register has a lowest possible value within the full sequence of gray-code values.

[c3] 3.The gray-code error corrector of claim 2 wherein the first differing bit-position is bit-position M, wherein M is a whole number and a lowest bit-position is position zero;

wherein the low-bit generator generates N low bits when the differing-bit searcher is not activated, but generates M low bits when the differing-bit searcher is activated.

[c4] 4.The gray-code error corrector of claim 3 further comprising:

a re-activation controller, activated once the stored register is loaded, for re-activating the full comparator to compare the input gray-code word to the corrected gray-code word in the stored register after loading;

wherein successively-loaded values in the stored register are re-compared until the input gray-code word matches the corrected gray-code word in the stored register, whereby comparison and loading of the stored register are repeated until the corrected gray-code word matches the input gray-code word.

- [c5] 5.The gray-code error corrector of claim 4 wherein the stored register is loaded in response to a clock; wherein the re-activation controller re-activates the full comparator in response to the clock, whereby comparison and loading of the stored register are repeated in response to the clock.
- [c6] 6.The gray-code error corrector of claim 5 wherein M is reduced on successive clock cycles of the clock when the input gray-code word does not change for the successive clock cycles; wherein the corrected gray-code word becomes more accurate on the successive clock cycles, whereby the corrected gray-code word converges over the successive clock cycles to accurately track the input gray-code word.
- [c7] 7.The gray-code error corrector of claim 5 further comprising:  
sample means, coupled to the input, for sampling the input in response to a receiver clock that differs from a transmitter clock, the input gray-code words being transmitted synchronously with the transmitter clock but sampled asynchronously by the receiver clock;  
wherein when the transmitter clock is faster than the receiver clock, not all gray-code words in the received se-

quence are sampled;  
wherein the input gray-code word and the corrected gray-code word differ by more than the maximum of N bits when the transmitter clock is faster than the receiver clock.

[c8] 8.The gray-code error corrector of claim 7 wherein the clock that loads the stored register is the receiver clock or a derivative of the receiver clock.

[c9] 9.A method for correcting transmission errors comprising:  
receiving from a transmission medium a received codeword encoded using a gray code, the received codeword having a most-significant-bit (MSB) portion and a least-significant-bit (LSB) portion, the MSB portion being a received MSB and the LSB portion being a received LSB;  
maintaining a stored codeword encoded using the gray code, the stored codeword having a stored MSB and a stored LSB;  
comparing the received MSB to the stored MSB;  
when the received MSB is different than the stored MSB, generating a generated LSB such that a combination of the received MSB and the generated LSB is a lowest-possible value in a sequence of the gray code, and storing the generated LSB as the stored LSB and storing the received MSB as the stored MSB and repeating the

method upon a change of a clock;  
when the received MSB matches the stored MSB, comparing the received LSB to the received LSB to determine when the received codeword is larger than the stored codeword; and  
when the received codeword is larger than the stored codeword, and the received MSB matches the stored MSB, searching for a first mis-matching bit between the received LSB and the stored LSB, the first mis-matching bit dividing the received LSB into an upper matched portion and a lower mis-matched portion, and generating the generated LSB having the upper matched portion from the received LSB and a generated lower mis-matched portion such that a combination of the received MSB, the upper matched portion and the generated lower mis-matched portion is a lowest-possible value in a sequence of the gray code, and storing the upper matched portion and the generated lower mis-matched portion as the stored LSB and repeating the method upon a change of the clock,  
whereby transmission errors are corrected by generating lower bits of the stored codeword.

- [c10] 10. The method of claim 9 wherein the method is repeated for each change of the clock even when the received codeword does not change.

- [c11] 11.The method of claim 9 wherein the received codeword and the stored codeword each comprise L bits; wherein the stored LSB and the received LSB each comprise N bits; wherein the stored MSB and the received MSB each comprise L-N bits, wherein L and N are whole numbers and L is greater than N.
- [c12] 12.The method of claim 10 wherein successive codewords sent over the transmission medium are increasing in value or remaining at a same value in a sequence of the gray code.
- [c13] 13.The method of claim 12 wherein successive codewords sent over the transmission medium can increase by a maximum of  $2^N - 1$  and have a maximum of N bits change between successive codewords.
- [c14] 14.The method of claim 11 wherein a multi-bit change of N bits in the received codeword cause the stored codeword to converge to a correct value over a maximum of N-1 extra cycles of the clock.
- [c15] 15.The method of claim 11 wherein a bit-position of the first mis-matching bit becomes less significant in position over N-1 extra cycles of the clock when the stored

codeword is converging.

- [c16] 16. The method of claim 9 further comprising:  
receiving a sequence of signals representing a new codeword from a transmitter over the transmission medium;  
updating with the new codeword the received MSB and the received LSB of the received codeword in a received register upon the change of the clock; and  
updating the stored MSB and the stored LSB upon the change of the clock.
- [c17] 17. An error-correcting receiver comprising:  
received word means, coupled to receive an input gray-code word, the received word means having an upper received-word of upper received bits of the input gray-code word, and a lower received-word of N lower received bits of the input gray-code word;  
wherein successively-received input gray-code words differ by a maximum of N bits, wherein N is a whole number of two or more;  
stored register means for storing a corrected gray-code word, the stored register means having an upper portion that stores upper stored bits and a lower portion that stores N lower stored bits of the corrected gray-code word;  
upper comparator means, coupled to the received word

means and to the stored register means, for comparing the upper received bits to the upper stored bits;  
upper loader means, activated by the upper comparator means when the upper received bits and the upper stored bits mis-match, for copying the upper received bits into the upper portion of the stored register means;  
low-bit generator means for generating lower stored bits for loading into the lower portion of the stored register means such that the stored register means has a lowest possible value within a sequence of gray-code values after loading;  
full compare means, coupled to the received word means and to the stored register means, for comparing the input gray-code word to the corrected gray-code word;  
and  
differing-bit search means for locating a first differing bit-position and loading bits above the first differing bit-position from the received word means into the stored register means and generating lowest-possible low bits for storage in the stored register means below the first differing bit-position.

- [c18] 18. The error-correcting receiver of claim 17 further comprising:  
control means for activating the full compare means and the differing-bit search means, wherein the full compare

means is activated when the upper comparator means determines that the upper received bits match the upper stored bits; and

wherein the differing-bit search means is activated when the upper comparator means determines that the upper received bits match the upper stored bits and when the full compare means determines that the input gray-code word is larger than the corrected gray-code word.

[c19] 19. The error-correcting receiver of claim 18 further comprising:

clock means, for loading the stored register means in response to a clock, and for re-activating the full compare means to compare the input gray-code word to the corrected gray-code word in the stored register means after loading;

wherein loaded-loaded values in the stored register means are re-compared until the input gray-code word matches the corrected gray-code word in the stored register means,

whereby comparison and loading of the stored register means are repeated until the corrected gray-code word matches the input gray-code word.

[c20] 20. The error-correcting receiver of claim 19 further comprising:

line input means, coupled to the received word means,

for receiving the input gray-code words in a received sequence over a communications line, the input gray-code words belonging to a full sequence of gray-code values, wherein successive gray-code values in the full sequence have only one bit difference, wherein the received sequence contains successively-received words that differ by a maximum of N bits, wherein N is a whole number of two or more, wherein the successively-received words differ in value by a maximum of  $2^N - 1$ .